Description of one of Crosetto's innovative concepts that enables acquiring data at a very high input rate while simultaneously allowing necessary time to accurately analyze the information

The figure on the right shows the flow of data during twelve clock cycles in an electronic channel of the 3D-Flow parallel-processing system, that, at each clock, acquires a data set as input and provides a result as output, allowing a processing time for each data set, in each layer, for a time longer than the time interval between two consecutive input data sets.

Each layer of the 3D-Flow parallel-processing system consists of an array of processor with fast bidirectional data exchange capabilities between adjacent processors within the array (North, East, West, South –NEWS-).

The entire algorithm must be executed from start to finish in each 3D-Flow processor in order to exchange data with adjacent processors and keep consistency with the same set of input data.

Processors at the same x-y location in arrays at different layers are connected via Top-Bottom ports (as shown in the figure) to form an electronic channel.

In the example, a 3D-Flow processor is replicated five times in the 3D-Flow parallel-processing system.(The number of times the 3D-Flow processor is copied is equal to the ratio between the maximum algorithm execution time and the time interval between two consecutive sets of input data).

The figure shows an example where the maximum algorithm execution time is 500 nanoseconds and the time interval between two consecutive sets of input data is 100 nanoseconds. (Thus it is: 500/100 = 5).

A 3D-Flow processor is represented in the figure with three functions: a) a "bypass switch" to bypass data, represented as a long arrow in a rectagular box, b) a "bypass register" that is an output register, represented as a rectangular to the right of the arrow and c) a CPU or Central Processing Unit, represented as a rectangul below the arrow.

A "bypass switch" sends a set of data to its CPU and transfers ("bypasses") four sets of data to the next layers to the right in the figure.

Time	Proc (1d)	Reg (1d)	Proc (2d)	Reg (2d)	Proc (3d)	Reg (3d)	Proc (4d)	Reg (4d)	Proc (5d)	Reg (5d)
1t	1									
2t	1	i2								
3t	1	i3	2							
4t	1	i4	2	i3						
5t	1	i5	2	i4	3					
6t	6	r1	2	i5	3	i4				
7t	6	i7	2	r1	3	i5	4			
8t	6	i8	7	r2	3	r1	4	i5		
9t	6	i9	7	i8	3	r2	4	r1	5	
10t	6	i10	7	i9	8	r3	4	r2	5	r1
11t	11	r6	7	i10	8	i9	4	r3	5	r2
12t	11	i12	7	r6	8	i10	9	r4	5	r3

Table 1 shows the sequence of the sets of data in different times in one 3D-Flow electronic channel. A set of data contains information received at a given time from a "detector channel" of the 3D-CBS detector.

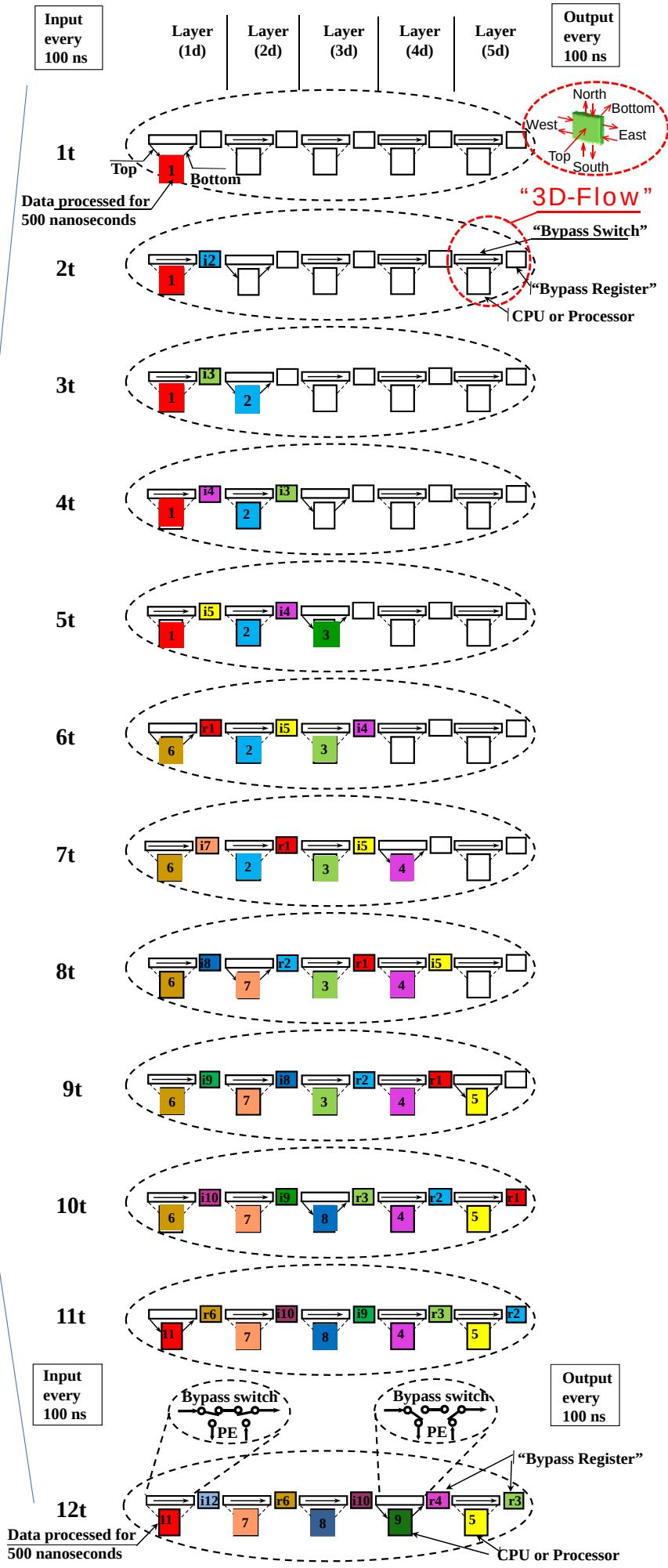
In the first column (on the left of the table) is shown the time "t". Values below the columns labeled with Proc (1d), Proc (2d), Proc (3d), Proc (4d), Proc (5d) represent the sets of data that are processed by the 3D-Flow processor in the specific "t" time.

Values labeled with ix and rx below columns Reg (1d), Reg (2d), Reg (3d), Reg (4d), Reg (5d) are input data and output results respectively, that flow from register to register in the electronic channel chain toward the exit point.

One should note that data-package No. 1 stays in the first processor of the first layer for five cycles, while four data sets (i2, i3, i4 and i5) are passed forward (via the "bypass switch") to the next layer.

For example at clock 6t, while processor 1d receives data set No. 6, at the same time it outputs results r1 relative to the data processed previously. This result "r1" is then transferred to the output of the 3D-Flow system without being processed by other layers.

One should note that input data and output results in the 3D-Flow system are intercalated in such a way that on the left there are only input data, on the right only results and in the center are intercalated, increasing the number of results toward the exit of the system.



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