TABLE III. SEQUENCE OF THE DATA PACKET AT DIFFERENT TIMES IN THE PIPELINE STAGE (SEE FIGURE 10). ONE DATA PACKET IN THIS APPLICATION CONTAINS 64-BIT INFORMATION FROM ONE CHANNEL OF THE PET DETECTOR. THE CLOCK TIME AT EACH ROW IN THE FIRST COLUMN OF THE TABLE IS EQUAL TO $t = (t_1 + t_2 + t_3)$ OF FIGURE 10. THE NUMBER IN THE LOWER POSITION IN A CELL OF THE TABLE IS THE NUMBER OF THE INPUT DATA PACKET THAT IS PROCESSED BY THE 3D-FLOW PROCESSOR AT A GIVEN STAGE. THE VALUES IN THE RAISED POSITION, INDICATED AS ix AND rx, ARE THE INPUT DATA AND THE RESULT DATA, RESPECTIVELY, WHICH FLOW FROM REGISTER TO REGISTER IN THE PIPELINE TO THE EXIT POINT OF THE SYSTEM. NOTE THAT INPUT DATA 1 REMAINS IN THE PROCESSOR AT STAGE 1d FOR FIVE CYCLES, WHILE THE NEXT FOUR DATA PACKETS ARRIVING (i2, i3, i4, AND i5) ARE PASSED ALONG (BYPASS SWITCH) TO THE NEXT STAGE. NOTE THAT AT CLOCK 14t, WHILE STAGE 4d IS FETCHING 9, IT IS AT THE SAME TIME, OUTPUTTING r4. THIS r4 VALUE IS THEN TRANSFERRED TO THE EXIT OF THE 3D-FLOW SYSTEM WITHOUT BEING PROCESSED BY ANY OTHER d STAGES. NOTE THAT CLOCK 14t SHOWS THE STATUS REPRESENTED IN FIGURE 10 AND THAT INPUT DATA AND OUTPUT RESULTS ARE INTERCALATED IN THE REGISTERS OF THE 3D-FLOW PIPELINED SYSTEM.

Time	Proc (1d)	Reg (1d)	Proc (2d)	Reg (2d)	Proc (3d)	Reg (3d)	Proc (4d)	Reg (4d)	Proc (5d)	Reg (5d)
3t	1									
4t	1	i2								
5t	1	i3	2							
6t	1	i4	2	i3						
7t	1	i5	2	i4	3					
8t	6	r1	2	i5	3	i4				
9t	6	i7	2	r1	3	i5	4			
10t	6	i8	7	r2	3	r1	4	i5		
11t	6	i9	7	i8	3	r2	4	r1	5	
12t	6	i10	7	i9	8	r3	4	r2	5	r1
13t	11	r6	7	i10	8	i9	4	r3	5	r2
14t	11	i12	7	r6	8	i10	9	r4	5	r3

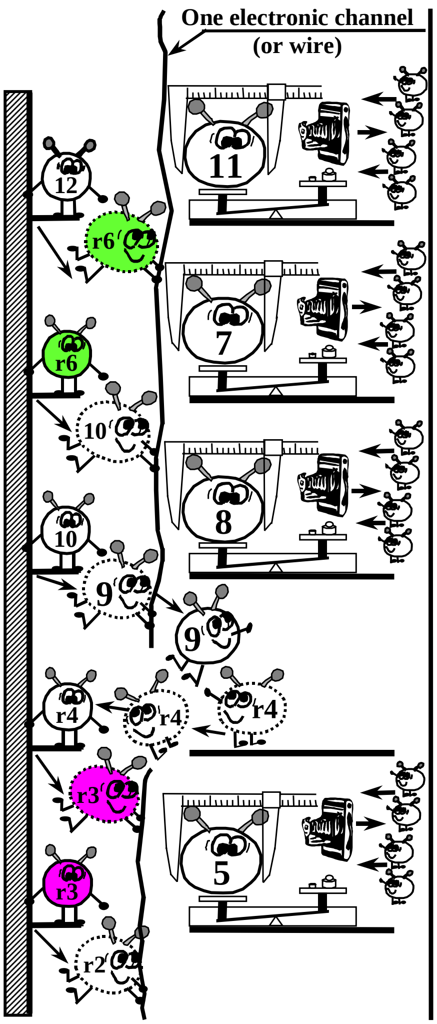

Figure 9. A "family reunion" cartoon for time 14t of Table III and Figure 10. Each photon remains in the measuring station (processor) for a duration five times longer than the time interval between two consecutive input data. The result from any measuring station will not be an input to the next station (as it is in a typical pipeline system) but will be passed on with no further processing in the 3D-Flow sequentially implemented, parallel-architecture until it exits (see additional description on next page).

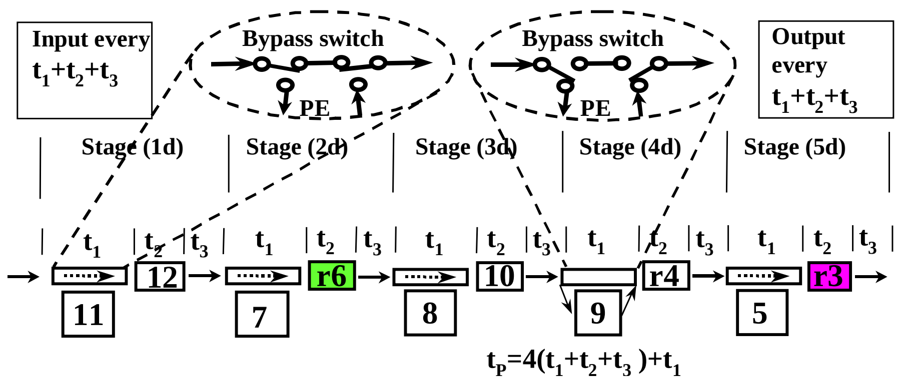

Figure 10. The example shows how the 3D-Flow system extends the execution time in a pipeline stage beyond the time interval between two consecutive input data (sequentially-implemented, parallel architecture). An identical circuit (a 3D-Flow processor) is copied 5 times at stage d (the number of times the circuit is copied corresponds to the ratio between the algorithm execution time and the time interval between two consecutive input data). A bypass switch (or multiplexer) coupled to each processor in each 3D-Flow stage 1d, 2d, 3d, 4d, and 5d sends one data packet to its processor and passes four data packets along to the next stage ("bypass switch"). Thus, the execution time at each substation d will be $t_P = 4(t_1 + t_2 + t_3) + t_1$. The numbers in the rectangles below the switches identify the input data packets to the CPU of the 3D-Flow processor. (See also Table III for the sequence of operations during the previous clock cycles). A 3D-Flow processor is shown in the figure with the three functions of (a) a bypass switch (dotted right arrow in the rectangle), (b) an output register (rectangle to the right), and (c) a CPU (rectangle below). See the practical implementation of the 3D-Flow architecture on Figure 27, Figure 28, Figure 29.